bridge member is aligned with the internal void, and wherein the substrate provides at least one wall that at least partially defines the void; and

a1 (concluded)

(d) etching through the second layer of the wafer around the periphery of the bridge member to break through into the [recess] void, thereby releasing the bridge from the substrate.

13. (Once Amended) The method as recited in claim 12, further comprising thinning the wafer such that the alignment hole extends entirely through the wafer.

14. (Once Amended) The method as recited in claim 1, wherein step (d) further comprises forming a stationary conductive member extending from the substrate that is separated from the bridge via a variable size gap.

a2

15. (Cancelled)

16. (Once Amended) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer having at least a first member and a second member;

(b) removing a portion of the first member through to the second member to form a bridge and a pair of spacers defining a recess therebetween;

(c) attaching the spacers to a substrate to form a composite structure having an internal void formed therein, wherein the bridge is aligned with the internal void, and wherein the substrate provides at least one wall that at least partially defines the internal void; and

(d) etching through the second member around the periphery of the bridge to break through into the recess and release the second member from mechanical communication with the substrate.

17. (Once Amended) The method as recited in claim 16, further comprising etching an alignment hole through the first, and second members and substantially through the wafer.

18. (Once Amended) The method as recited in claim 17, further comprising thinning the wafer such that the alignment hole extends entirely through the wafer.

a3

23. (Once Amended) The method as recited in claim 16, wherein step (d) further comprises forming a stationary conductive member extending from the substrate that is separated from the bridge via a variable size gap

24. Cancelled

28. (Once Amended) The method as recited in claim 16, wherein the substrate is selected from the group consisting of glass, high resistivity silicon, crystalline sapphire, crystalline silicon, polycrystalline silicon, silicon carbide, or ceramic.

a4

29. (Once Amended) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer;

(b) forming a pair of spacers at opposite ends of a surface of the wafer, wherein the spacers define a recess therebetween;

(c) depositing a layer onto the wafer in the recess;

(d) etching a portion of the layer to define a bridge;

(e) attaching the spacers to a substrate to define an internal void; and

(f) etching through the wafer into the void around the periphery of the bridge to release the bridge from mechanical communication with the substrate.

a5

32. (Once Amended) The method as recited in claim 29, wherein step (f) further comprises producing a stationary conductive MEMS element separated from the bridge via a variable size gap.

33. Cancelled

a6

39. (Once Amended) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer having at least a first and a second layer;

(b) etching into the first layer to produce a bridge;

(c) providing a substrate;

(d) etching a recess into a surface of the substrate;

(e) after step (b), attaching the wafer to the surface of the substrate to form an internal void such that the bridge is 1) disposed between the surface and the second layer, and 2) aligned with the void; and

a6 (concluded)

(f) etching through the second layer around the periphery of the bridge to release the bridge from mechanical communication with the substrate.

a7

48. (Once Amended) The method as recited in claim 39, wherein step (f) further comprises producing a stationary conductive MEMS element attached to the substrate separated from the bridge via a variable size gap.

49. Cancelled

50. Cancelled

a8

51. (Once Amended) The method as recited in claim 39, further comprising etching an alignment hole through the first and second layers, and partially through the wafer.

52. (Once Amended) The method as recited in claim 51, further comprising thinning the wafer such that the alignment hole extends entirely through the wafer.

53. (New) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer having at least a first layer and a second layer;

(b) removing a portion of the first layer to form a bridge member;

(c) after step (b), attaching the wafer to a substrate to form a composite structure having an internal void formed therein, wherein the bridge member is aligned with the internal void; and

(d) etching through the second layer of the wafer around the periphery of the bridge member to break through into the void, thereby releasing the bridge from the substrate and forming a conductive member extending from the bridge separated from a stationary member by a variable size gap.

54. The method as recited in claim 53, further comprising depositing a conductive layer onto the wafer.

55. (New) The method as recited in claim 54, wherein the conductive layer is selected from the group consisting of aluminum, copper, silver, gold and nickel.

A8 (continued)

56. (New) The method as recited in claim 53, wherein the wafer is selected from the group consisting of silicon, silicon carbide and gallium arsenide.

57. (New) The method as recited in claim 53, wherein the substrate is a non-conductive substrate selected from the group consisting of glass, high resistivity silicon, crystalline sapphire, and ceramic.

58. (New) The method as recited in claim 53, wherein the substrate is a conductive substrate selected from the group consisting of silicon, silicon carbide, and gallium arsenide.

59. (New) The method as recited in claim 53, wherein the void is formed by pre-patterning a recess into a surface of the wafer prior to step (c), and bonding the surface to the substrate.

60. (New) The method as recited in claim 53, wherein the void is formed by pre-patterning a recess into a surface of the substrate prior to step (c), and bonding the surface to the wafer.

61. (New) The method as recited in claim 53, wherein the recess has beveled edges.

62. (New) The method as recited in claim 53, wherein the bridge member comprises an insulating material.

63. (New) The method as recited in claim 62, wherein the bridge member comprises silicon dioxide.

64. (New) The method as recited in claim 53, further comprising etching an alignment hole into the wafer.

65. (New) The method as recited in claim 64, further comprising thinning the wafer such that the alignment hole extends entirely through the wafer.

66. (New) The method as recited in claim 53, wherein step (d) further comprises forming the stationary member extending outwardly from the substrate.

67. (New) The method as recited in claim 53, wherein the conductive member and stationary member are electrically isolated from one another.

68. (New) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer having at least a first member and a second member;

(b) removing a portion of the first member to form a bridge and a pair of spacers defining a recess therebetween;

A8 (continued)

(c) attaching the spacers to a substrate to form a composite structure having an internal void formed therein, wherein the bridge is aligned with the internal void; and

(d) etching through the second member around the periphery of the bridge to break through into the recess and release the second member from mechanical communication with the substrate, wherein the etching step forms a conductive member extending from the bridge and separated from a stationary member via a variable size gap.

69. (New) The method as recited in claim 68, further comprising etching an alignment hole through the first, and second layers and substantially through the wafer.

70. (New) The method as recited in claim 69, further comprising thinning the wafer such that the alignment hole extends entirely through the wafer.

71. (New) The method as recited in claim 68, wherein the first member comprises a first layer and a second layer of selectively etchable materials, wherein the first layer is etched to form the spacers, and wherein the second layer is etched to form the bridge.

72. (New) The method as recited in claim 71, wherein the second layer is made of an insulating material.

73. (New) The method as recited in claim 72, wherein the second layer comprises silicon dioxide.

74. (New) The method as recited in claim 71, wherein the first layer is selected from the group consisting of silicon nitride and polycrystalline silicon.

75. (New) The method as recited in claim 68, wherein step (d) further comprises forming the stationary member extending outwardly from the substrate.

76. (New) The method as recited in claim 68, wherein the conductive member and stationary member are electrically isolated from one another.

A8 (continued)

77. (New) The method as recited in claim 68, wherein the second member comprises silicon.

78. (New) The method as recited in claim 68, further comprising depositing and patterning a conductive layer onto the first layer.

79. (New) The method as recited in claim 78, wherein the conductive layer comprises aluminum.

80. (New) The method as recited in claim 68, wherein the substrate is selected from the group consisting of glass, high resistivity silicon, crystalline sapphire, crystalline silicon, polycrystalline silicon, silicon carbide, or ceramic.

81. (New) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer;

(b) forming a pair of spacers at opposite ends of a surface of the wafer, wherein the spacers define a recess therebetween;

(c) depositing a layer onto the wafer in the recess;

(d) etching a portion of the layer to define a bridge;

(e) attaching the spacers to a substrate to define an internal void; and

(f) etching through the wafer into the void around the periphery of the bridge to release the bridge from mechanical communication with the substrate and to produce a stationary conductive MEMS element attached to the substrate, and a movable conductive MEMS element supported by the bridge.

82. (New) The method as recited in claim 81, wherein the layer is insulating.

83. (New) The method as recited in claim 82, wherein the layer comprises silicon dioxide.

84. (New) The method as recited in claim 81, wherein the conductive member and stationary member are electrically isolated from one another.

85. (New) The method as recited in claim 81, further comprising depositing a conductive layer onto the wafer.

A8 (continued)

86. (New) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer;

(b) partially etching into a surface of the wafer to form a recess therein disposed between a pair of spacers;

(c) depositing a layer onto the surface of the wafer in the recess so as to form a bridge;

(d) attaching the spacers to a substrate to define an internal void; and

(e) etching through the wafer into the void around the periphery of the bridge to release the bridge from mechanical communication with the substrate and to produce a stationary conductive MEMS element attached to the substrate, and a movable conductive MEMS element supported by the bridge and separated by the stationary element via a variable size gap.

87. (New) The method as recited in claim 86, wherein the layer is insulating.

88. (New) The method as recited in claim 87, wherein the layer comprises silicon dioxide.

89. (New) The method as recited in claim 86, further comprising depositing a conductive layer onto the wafer.

90. (New) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer having at least a first and a second layer;

(b) etching into the first layer to produce a bridge;

(c) providing a substrate;

(d) etching a recess into a surface of the substrate;

(e) after step (b), attaching the wafer to the surface of the substrate to form an internal void such that the bridge is 1) disposed between the surface and the second layer, and 2) aligned with the void; and

(f) etching through the second layer around the periphery of the bridge to release the bridge from mechanical communication with the substrate and to produce a stationary conductive MEMS element attached to the substrate, and a movable conductive MEMS element supported by the bridge.

91. (New) The method as recited in claim 90, further comprising depositing a conductive layer onto the wafer.

A8 (continued)

92. (New) The method as recited in claim 91, wherein the conductive layer is selected from the group consisting of aluminum, copper, silver, gold and nickel.

93. (New) The method as recited in claim 90, wherein the wafer is selected from the group consisting of silicon, silicon carbide and gallium arsenide.

94. (New) The method as recited in claim 90, wherein the substrate is a non-conductive substrate selected from the group consisting of glass, high resistivity silicon, crystalline sapphire, and ceramic.

95. (New) The method as recited in claim 90, wherein the substrate is a conductive substrate selected from the group consisting of silicon, silicon carbide, and gallium arsenide.

96. (New) The method as recited in claim 90, wherein the recess has beveled edges.

97. (New) The method as recited in claim 90, wherein the bridge member comprises an insulating material.

98. (New) The method as recited in claim 97, wherein the bridge member comprises silicon dioxide.

99. (New) The method as recited in claim 90, wherein the conductive member and stationary member are electrically isolated from one another.

100. (New) The method as recited in claim 90, wherein step (f) further comprises forming a conductive member extending from the bridge and separated from a stationary member via a variable size gap.

a8 (concluded)

101. (New) The method as recited in claim 90, further comprising etching an alignment hole through the first and second layers, and partially through the wafer.

102. (New) The method as recited in claim 101, further comprising thinning the substrate such that the alignment hole extends entirely through the wafer.